Universal Chiplet Interconnect Express™ (UCIe™): An open standard for innovations at package level

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Agenda

• Introduction to UCIe
• On-Package Interconnects: Opportunities and Challenges
• Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets
• Future Directions and Conclusions
Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive The open chiplet ecosystem.

JOIN US!
UCIe Consortium is open for membership

• UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level**.

• **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

• **Contributor Membership**
  – Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  – Implement with the IP protections as outlined in the Agreements
  – Right to attend Corporation trade shows or other industry events as determined by the Board
  – Participate in the technical working groups
  – Influence the direction of the technology
  – Access the intermediate (dot level) specifications
  – Election to get to the Promoter Class/ Board every year when the term of half the board completes

• **Adopter Membership**
  – Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  – Implement with the IP protections as outlined in the Agreements
  – Right to attend Corporation trade shows or other industry events as determined by the Board
Agenda

- Introduction to UClE
- On-Package Interconnects: Opportunities and Challenges
- Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets
- Future Directions and Conclusions
Moore Predicted “Day of Reckoning”

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

-Gordon E. Moore

¹: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965
Drivers for On-Package Chiplets

- Reticle Limit, yield optimization, scalable performance
  - Same dies on package (Scale-up)
- Increasing design costs at leading edge process nodes
  - Die-disaggregated dies across different nodes
  - Use new process node for advanced functionality
- Time to Market (Late binding)
- Custom silicon for different customers leveraging a base product
  - E.g., Different acceleration functions with common compute
- Different process nodes optimized for different functions
  - E.g., Memory, logic, analog, co-packaged optics
  - High power-efficient bandwidth with low-latency access (e.g., HBM memory)

Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)
Components of Chiplet Interoperability

- **Chiplet Form Factor**
  - Die size
  - Bump location
  - Power delivery
  - Thermal characteristics

- **SoC Construction** (Application Layer)
  - SoC Reset
  - Initialization (e.g., fuses)
  - Register access
  - Security

- **Die-to-Die Protocols** (Data Link to Transaction Layer)
  - Link Layer, transaction Layer, etc.: PCIe/ CXL/ Raw/...
  - Internal interface standardization for plug and play IPs

- **Die-to-Die I/O** (Physical Layer)
  - Bump arrangement and characteristics
  - Electrical & thermal characteristics
  - Substrate or interposer characteristics
  - Length budget, pJ/bit, bit error rate, ...
  - Reset, clocking, initialization, and data transfer
  - Test and repair
  - Technology transition → multiple bump arrangement/ frequency
Design Choice: Seamless Integration from Node ➔ Package ➔ On-die enables Reuse, Better User Experience

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale, time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!
Universal Chiplet Interconnect Express (UCIe):

An Open Standard for Chiplets

Guiding principles of UCIe

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)
Motivation for UCIe

Align Industry around an open platform to enable chiplet based solutions

- Enables SoC construction that exceeds maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)

- Reduces time-to-solution (e.g., enables die reuse)

- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost

- Enables a customizable, standard-based product for specific use cases (bespoke solutions)

- Scales innovation (manufacturing/ process locked IPs)
UCIe: Key Metrics and Adoption Criteria

Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost: Standard vs advanced packaging

Factors Affecting Wide Adoption

- Interoperability
  - Full-stack, plug-and-play with existing s/w
  - Different usages/segments - ubiquity
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

UCIe is architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria
UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCle and Streaming
  - **CXL™/PCle® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCle
    - CXL/PCle addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/ Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI, etc)
- **Well defined specification:** interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface

**Scope of UCIe Specification**

- **Logical View**
  - Protocol Layer
    - CXL, PCIe, Streaming (e.g., AXI, CHI, symmetric coherency, memory, etc)
  - Raw Mode
    - Bypass Die to Die Adapter to RDI — e.g., SERDES to SoC
- **Physical View**
  - Flit-Aware Die to Die Interface (FDI)
  - Raw Die to Die Interface (RDI)
  - Link Training
  - Lane Repair / Reversal
  - (De) Scrambling
  - Analog Front end/ Clocking
  - Sideband, Config Registers
  - Channel

- **Layered View**
  - Configuration register for discovery and run-time
  - (Bumps/ Bump Map)
UCle 1.0: Supports Standard and Advanced Packages

(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer

One UCle 1.0 Spec covers both type of packaging options
UCIe Usage Model: SoC at Package Level

- SoC as a Package level construct
  - Standard and/or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, etc
  - Similar to PCIe/ CXL at board level
Example Scale-up SoC from homogeneous dies: Large Switch with on-die protocol as streaming over UCIe

- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIe based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIe as d2d interconnect – while this is a scale-up CXL switch, a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIe rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology

One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIe using the same principle. Here the UCIe PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric.

Ack: Nathan Kalyanasundaram
Example Scale-up Package using Streaming and open-plug-in using PCIe/CXL

- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion.
- Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry.

Ack: Marvin Denman, Bruce Mathewson, Francisco Socal, Durgesh Srivastava, Dong Wei

(3 dies on one package)
UCle Usage: Off-Package Connectivity with UCle Retimers

(Vision: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/sharing as well as message passing)

(Pod of Racks) CXL Rack/Pod level connected using long-reach media (Electrical/Optical/...) through UCle Retimers (e.g., co-packaged optics)

(Physical Connectivity using UCle Retimer based co-packaged optics)

Rack/Pod Level resource pooling/sharing with UCle
### UCIe 1.0: Characteristics and Key Metrics

#### Characteristics / KPIs

<table>
<thead>
<tr>
<th>Characteristic / KPIs</th>
<th>Standard Package</th>
<th>Advanced Package</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate (GT/s)</td>
<td>4, 8, 12, 16, 24, 32</td>
<td></td>
<td>Lower speeds must be supported - interop (e.g., 4, 8, 12 for 12G device)</td>
</tr>
<tr>
<td>Width (each cluster)</td>
<td>16</td>
<td>64</td>
<td>Width degradation in Standard, spare lanes in Advanced</td>
</tr>
<tr>
<td>Bump Pitch (um)</td>
<td>100 – 130</td>
<td>25 - 55</td>
<td>Interoperate across bump pitches in each package type across nodes</td>
</tr>
<tr>
<td>Channel Reach (mm)</td>
<td>&lt;= 25</td>
<td>&lt;=2</td>
<td></td>
</tr>
</tbody>
</table>

#### KPIs / Target for Key Metrics

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</thead>
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<tr>
<td>B/W Shoreline (GB/s/mm)</td>
<td>28 – 224</td>
<td>165 – 1317</td>
<td>Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)</td>
</tr>
<tr>
<td>B/W Density (GB/s/mm²)</td>
<td>22-125</td>
<td>188-1350</td>
<td></td>
</tr>
<tr>
<td>Power Efficiency target (pJ/b)</td>
<td>0.5</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>Low-power entry/exit latency</td>
<td>0.5ns &lt;=16G, 0.5-1ns &gt;=24G</td>
<td></td>
<td>Power savings estimated at &gt;= 85%</td>
</tr>
<tr>
<td>Latency (Tx + Rx)</td>
<td>&lt; 2ns</td>
<td></td>
<td>Includes D2D Adapter and PHY (FDI to bump and back)</td>
</tr>
<tr>
<td>Reliability (FIT)</td>
<td>0 &lt; FIT (Failure In Time) &lt;&lt; 1</td>
<td></td>
<td>FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode</td>
</tr>
</tbody>
</table>

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years. Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.
Ingredients of broad inter-operable chiplet ecosystem

- Broad Market Manufacturing, Packaging and Test
- Chiplets & Chiplet Based Product Attach Points
- Thriving Chiplet Ecosystem
- Die-to-Die IPs, VIPs, Tools, and Methodologies
- Die-to-Die Open Industry Standards w/ compelling KPIs across wide usages

Well-defined Specs
(Electrical, Logical, Protocol (e.g., PCIe/ CXL) Software, Form-Factor, Management)

Test criteria based on Specs
(Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)

Test Tools And Procedures
Test H/W & S/W Validates
Test criteria
- Compliance
- Interoperability

PASS
(Clear Test Output)

Predictable path to design compliance with UCIe
Future Directions and Conclusions

Chiplets and D2D interface are essential to the compute continuum
- Power-efficient performance, yield optimization, different functions, custom solutions, cost-effective

UCIe standardization will propel the development an open ecosystem
- Open plug-and-play “slot” at package level will unleash innovations
- Evolution needs to track the underlying packaging technology to deliver compelling metrics
- Form-factor, New Protocols, and manageability are some other areas for innovation

The open chiplet journey with UCIe just started! Join us in what will be an exciting journey for decades!