Chiplet Ecosystem

Challenges and obstacles to overcome to reach chiplet nirvana

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Outline

- Why chiplets?
- Chiplet ecosystem
  - Principles
  - Challenges
  - Enablement
- Chiplet application
- Summary
Why Chiplets?

**Slowing of Moore’s Law**

- 2004
- 2007
- 2010
- 2013
- 2016
- 2019

**Increasing Cost**

- 45nm
- 32nm
- 28nm
- 20nm
- 14/16nm
- 7nm
- 5nm

**Reticle Limit**

- 2006
- 2009
- 2012
- 2014
- 2017
- 2020

**Die Size (MM²)**

- 100
- 1000

- Server CPU
- GPU

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[2] Cost per yielded mm² for a 250mm² die
### Choices Beyond Monolithic

<table>
<thead>
<tr>
<th>Feature</th>
<th>2.5D</th>
<th>3D</th>
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<tbody>
<tr>
<td>Small Die Yield; Avoid Reticle Size Limit</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Heterogeneous Integration</td>
<td>✓</td>
<td>✓</td>
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<td>Product Flexibility</td>
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<td>✓</td>
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<td>Latency</td>
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<td>Bandwidth</td>
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<td>Power</td>
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<td>Footprint</td>
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Chiplets Outlook

*DOMAIN SPECIFIC ACCELERATION TO MEET COMPUTE DEMAND*

- Need many kinds of compute
- Mix and match chiplets from many vendors
- Expect systems on packages with many forms of compute, memory and I/O integrated
- Reduces developmental cost and time to market

- AMD enables 3P chiplet integration through semi-custom business unit
- 2D and 3D integration are supported through Infinity Architecture
Chiplets are good

Chiplet ecosystem even better!

How do we get there?
Chiplet Ecosystem Enablement Pillars

- Widely adopted standard
- Vendor agnostic integration model

Emerging standard
- Universal Chiplet Interconnect Express (UCIe)
- Supported by multiple foundries, OSAT, hyperscalers, processor and device vendors
- 110 companies and growing

High-Speed Standardized Chip-to-Chip Interface (UCIe)

Custom Chiplets

Src: UCIe Consortium
Chiplet Ecosystem Challenges

- Standard integration model for all functions
  - Protocol/Electrical/Physical
  - Software/firmware
  - Security & Manageability
  - Debug and Test
  - Power/Thermal/RAS

- Additional challenges
  - Logistics
  - Mixing Foundries
  - System Test
Chiplet Attach/Usage Model

- PCIe/CXL device (well established)
  - Software/driver
  - Address translation
  - Error isolation and recovery
  - Use Case: Inference, video, crypto, compression or networking functions acceleration

- Memory Controller+PHY chiplets
  - Simple protocol desired for standardization
  - Streaming protocol supported for proprietary use case
  - Use Case: Flexible memory technology (HBM / DDR / LPDDR / G6 /..)

- Generic compute attach
  - HMM or other memory management instead of device ATS/ATC
  - Standard coherency architecture like CXL (simplified) or CHI
  - Holy Grail ?? Needs work and alignment in consortium

- SerDes I/O chiplets
  - Use case: Pcie 32G/64G/128G ; Ethernet 50G/100G/200G
Chiplet Footprint

- PCIe has several detailed Card Electro-Mechanical specifications
  - Defines sizes, speed and power requirements
  - CEM AIC, M.2 and U.2

- Chiplets also need form factor standards
  - Power, Width & Height
  - Links (BW), Beach front & Alignment
  - Etc.

- System In a Package (SiP) has significantly reduced flexibility than add-in cards
  - Standard Packages are more a bit more flexible than AP

- Structural dies may be required when there are holes or gaps between chiplets

- Form factor standardization is crucial for a chiplet ecosystem!
Package Resources & Impact

- Typically, many package resources are allocated for external IO and logic power delivery

- Chiplet interconnects are
  - Buried deep in the interior of the dies
  - Designed to be small (and coexist with SoC Logic)
  - Ideal chiplet interconnects will leverage available digital supplies
  - Chiplets expected to be deployed in harsh environments
  - Operating on noisy supplies, pushes solutions to be wide and slow

- UCIe allows multi-module(ganged) configurations for higher bandwidth

- Need good measurement and debug capabilities

UCIe only defines interconnect beach front
Power Delivery and DFX pins equally important
Chiplet Ecosystem Solution Stack

**PCIE/CXL DEVICE INTEGRATION MODEL**

- Two independent hardware stack
  - Protocol and Control
- Die management unit (DMU)
  - Hardware + Firmware
- Standard control and management software interface
- Platform specific firmware
- UCIe starting to tackle software interfaces

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**Production Testing**

**Scalable Design Verification/Platform Emulation**

**Runtime RAS, Security**

**Manageability (SPDM/MCTP)**

**Runtime FW operation (Power, Thermal, Management/Telemetry)**

**Chiplet FW authentication**

**Secure Boot/ Reset / Repair**

**DMU (Die Management Unit)**

**D2D Control**

**D2D Protocol**

**D2D Adapter**

**D2D Physical Layer**

**SW Stack (Command Processor, Accelerator driver)**

**Accelerator Interface**
Chiplet Applications

- Scalable CXL switch for illustration
  - Cost benefits due to standardized bridge chips
  - Flexibility to add
    - co-packaged optics
    - in-package memory
  - Many product options with a single die

128 lanes electrical
128 lanes equivalent optical
In-package memory
Summary

- Wide adoption of standard is critical
  - UCIe clears the bar with over 110 companies within 6 months of incorporation
  - UCIe on a path to enable multiple protocols – CXL, AXI, etc.
- PCIe/CXL device integration model is well established
- Critical for partners to collaborate closely
- May need custom solutions to kick start ecosystem
- Chiplets are here but will take a few years for an ecosystem
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