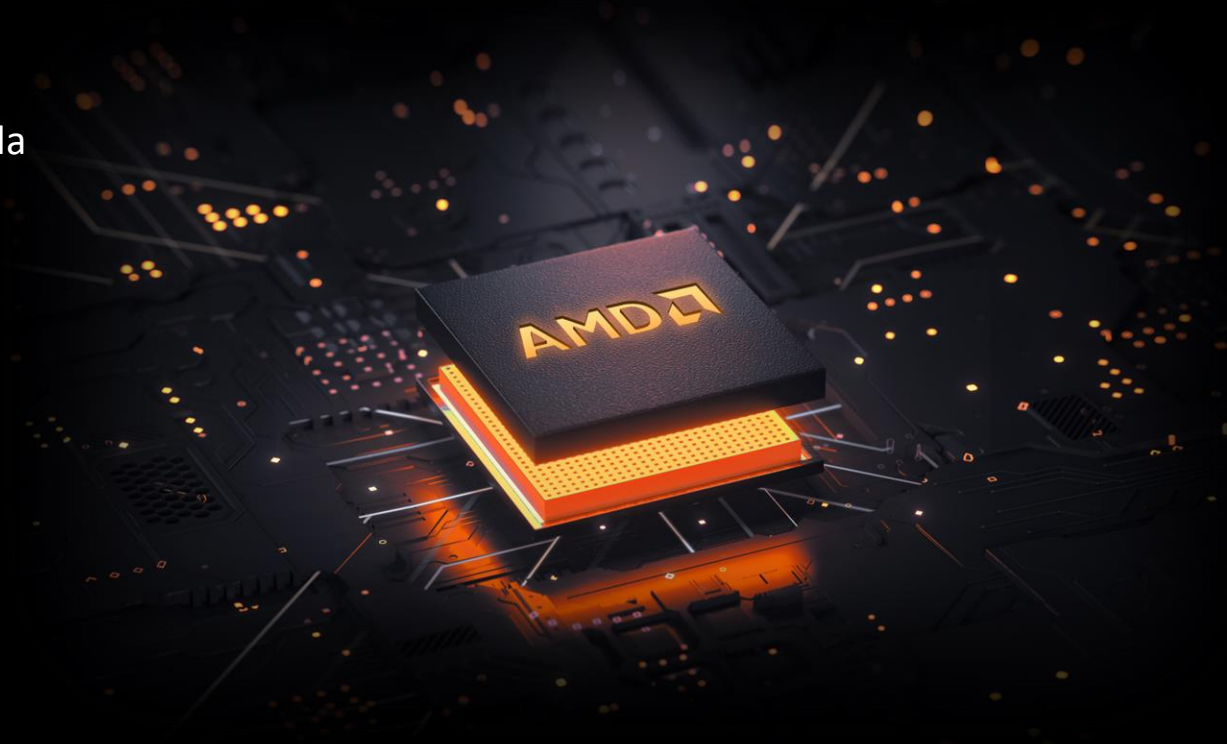
Chiplet Ecosystem

Challenges and obstacles to overcome to reach chiplet nirvana

The 2nd International HiPChips Workshop, HPCA 2023, Montreal, Canada



Nathan Kalyanasundharam & John Wuu

Advanced Micro Devices

Feb 26th, 2023

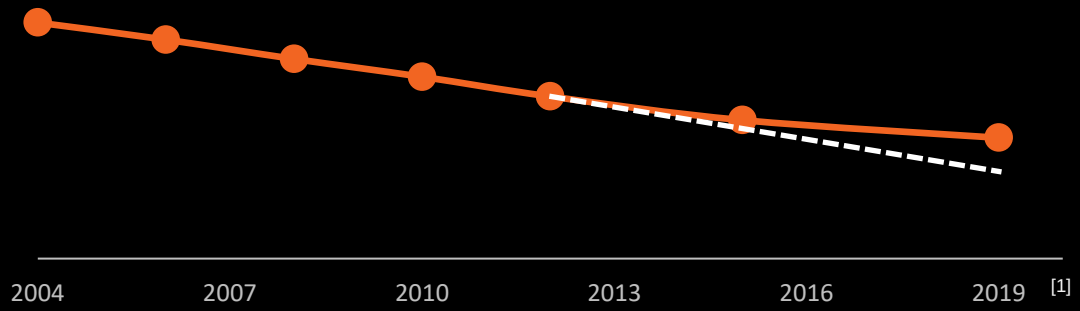
AMD

Outline

- Why chiplets?
- Chiplet ecosystem
  - Principles
  - Challenges
  - Enablement
- Chiplet application
- Summary

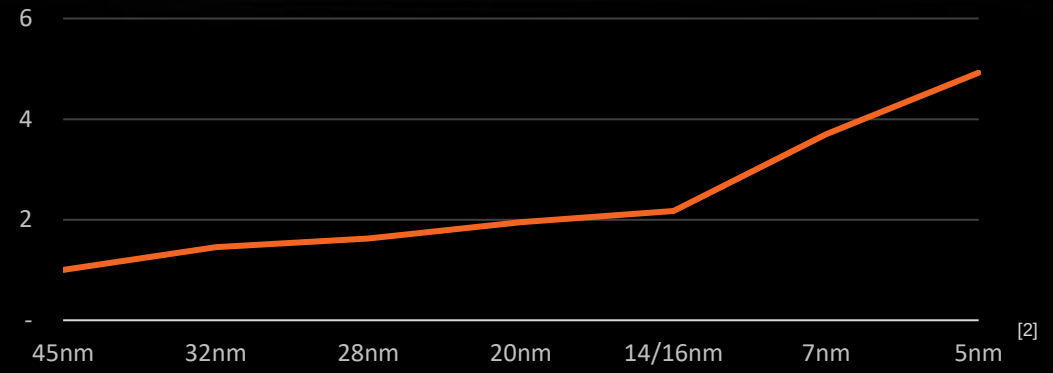
Why Chiplets?

Slowing of Moore's Law



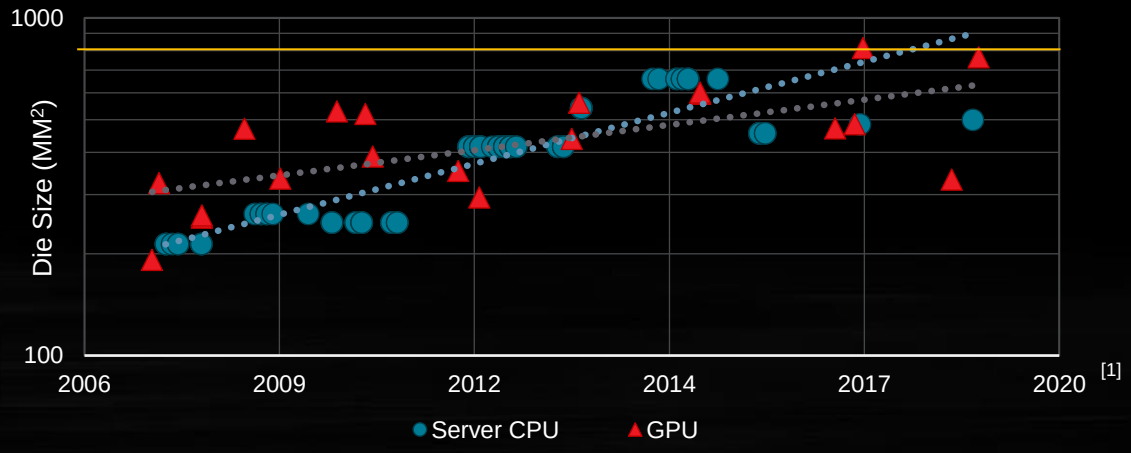
[1]

Increasing Cost

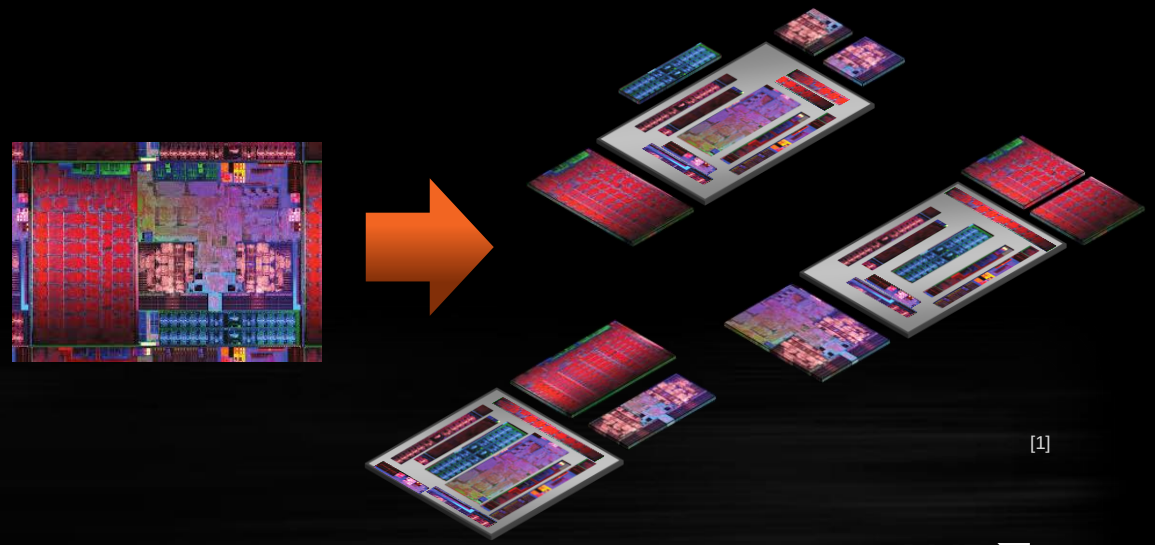


[2]

Reticle Limit



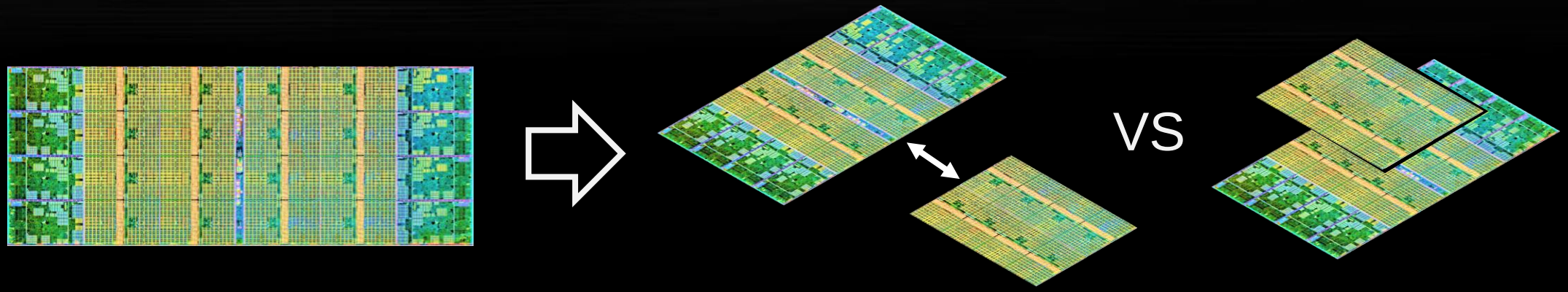
[1]



[1]

[1] Naffziger, VLSI Short Course, 2020, [2] Cost per yielded mm² for a 250mm² die

Choices Beyond Monolithic



	2.5D	3D
Small Die Yield; Avoid Reticle Size Limit	✓	✓
Heterogeneous Integration	✓	✓
Product Flexibility	✓	✓
Latency		✓
Bandwidth		✓
Power		✓
Footprint		✓

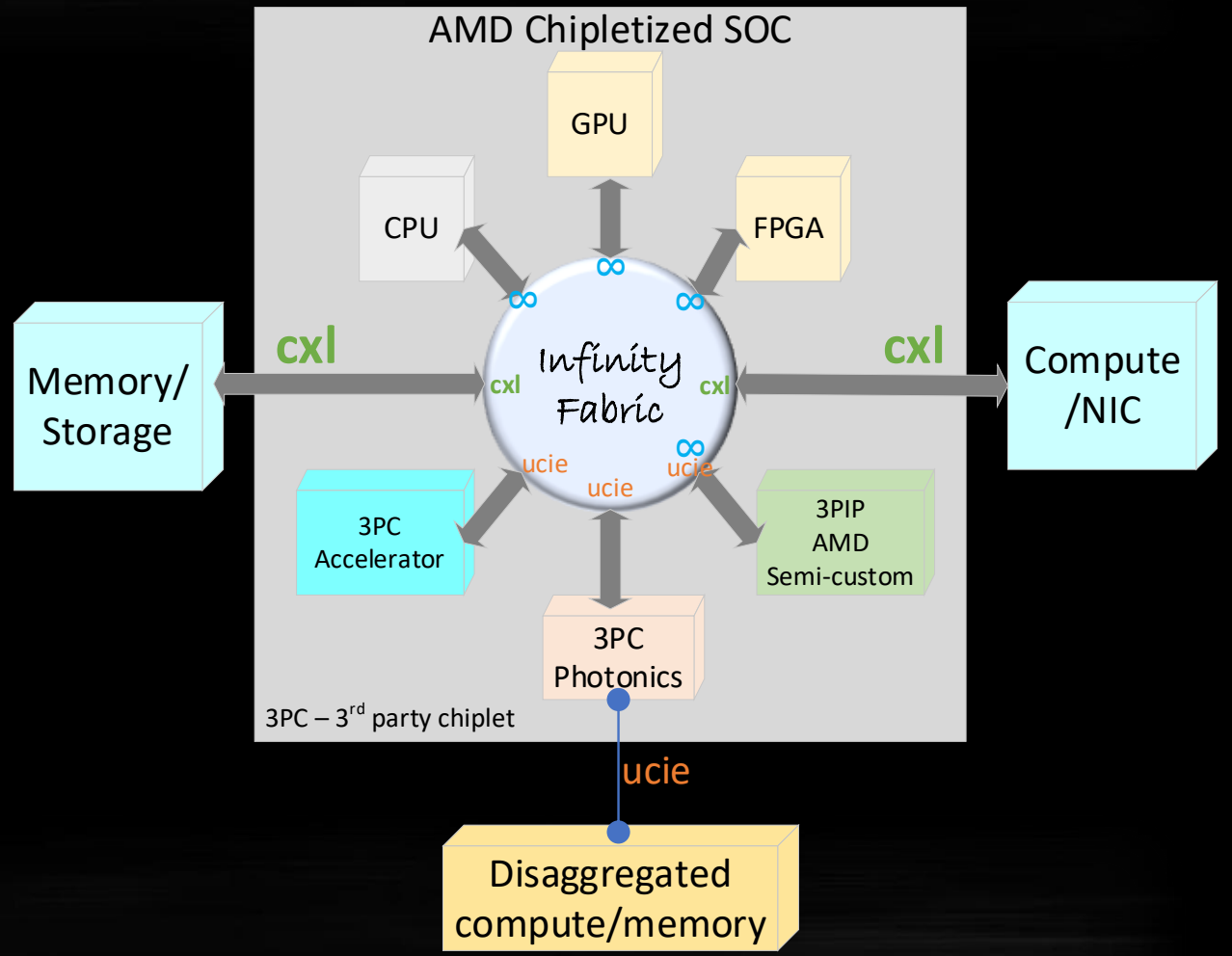
Wuu, IEDM Short Course, 2022

Chiplets Outlook

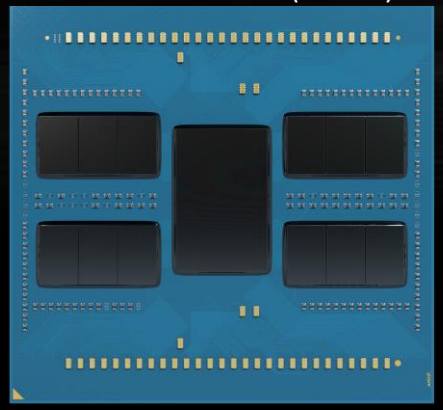
DOMAIN SPECIFIC ACCELERATION TO MEET COMPUTE DEMAND

- Need many kinds of compute
- Mix and match chiplets from many vendors
- Expect systems on packages with many forms of compute, memory and I/O integrated
- Reduces developmental cost and time to market

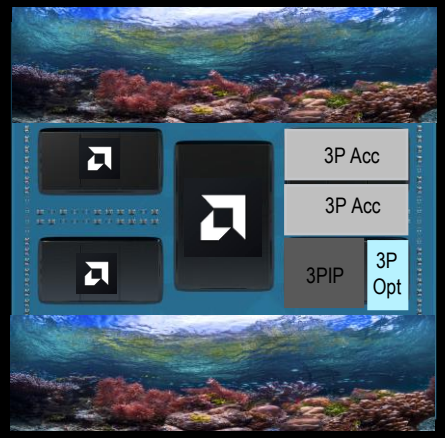
- AMD enables 3P chiplet integration through semi-custom business unit
- 2D and 3D integration are supported through Infinity Architecture



AMD 4th Gen EPYC (Genoa)



Chiplets are good



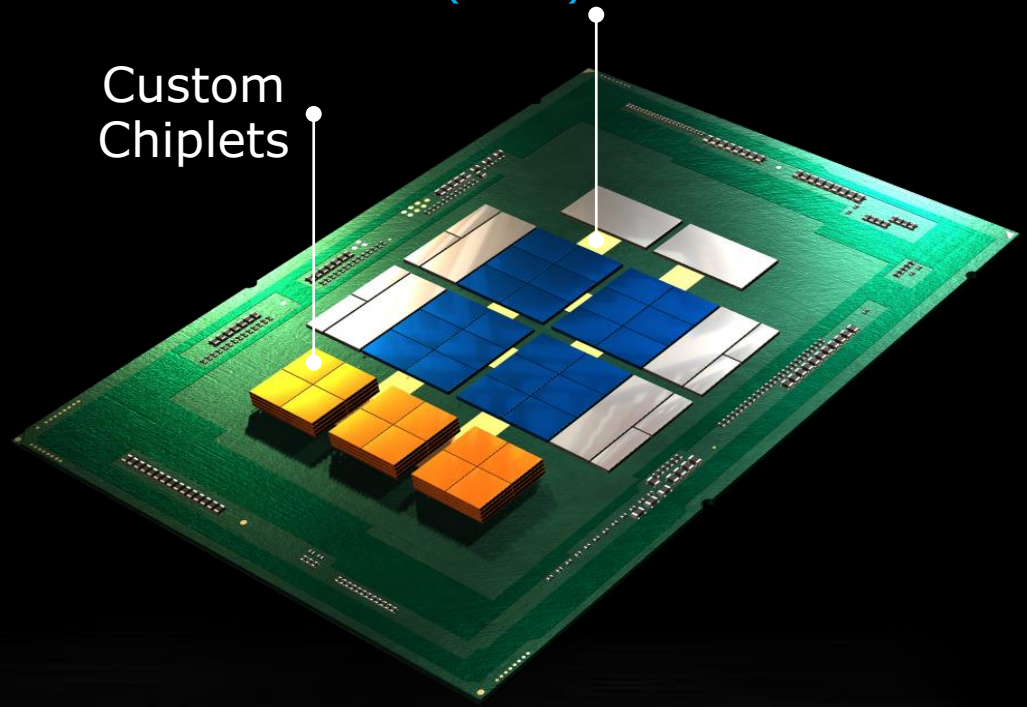
Chiplet ecosystem even better!

How do we get there?

Chiplet Ecosystem Enablement Pillars

- Widely adopted standard
- Vendor agnostic integration model

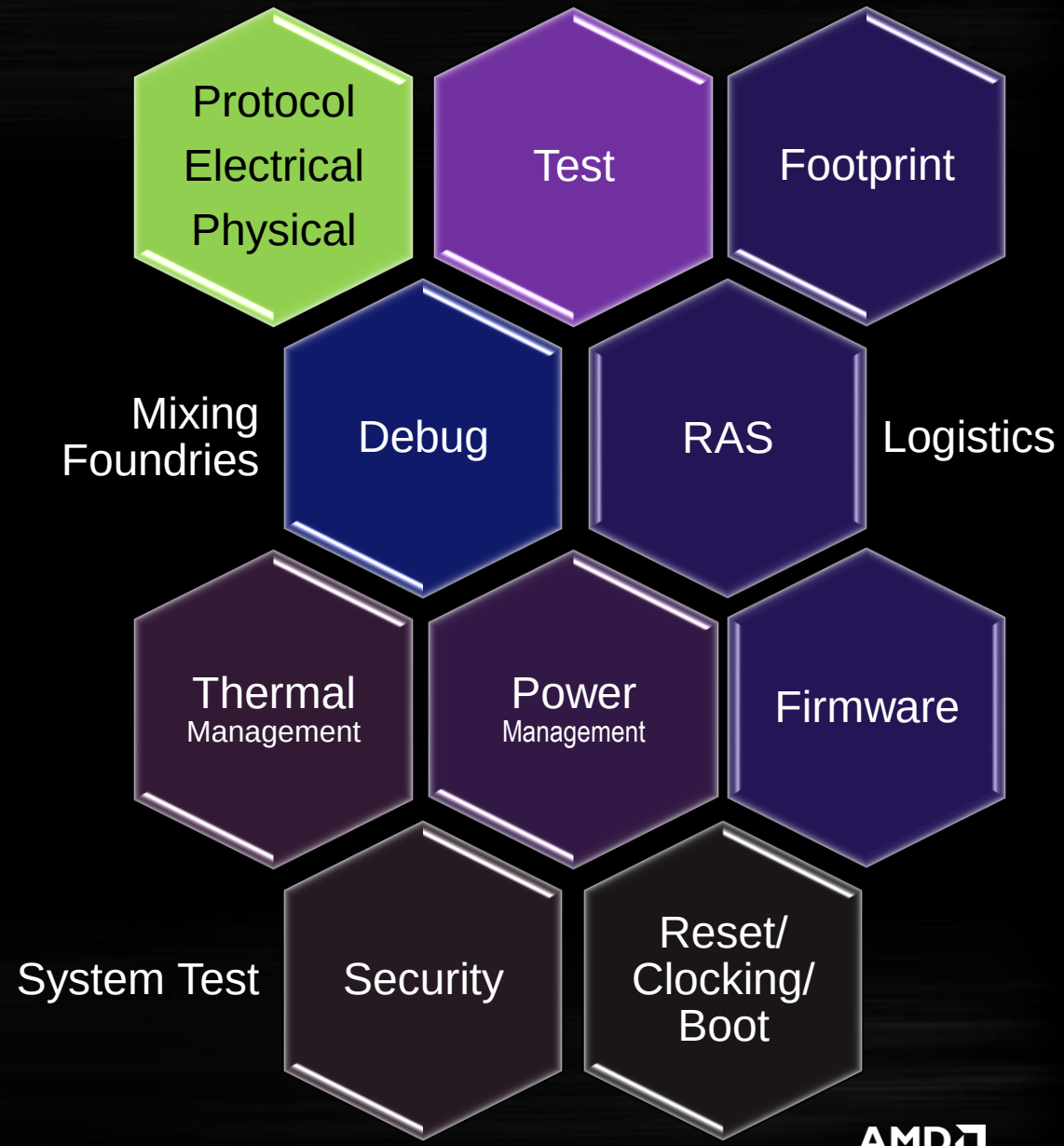
- Emerging standard
  - Universal Chiplet Interconnect Express (UCIe)
  - Supported by multiple foundries, OSAT, hyperscalars, processor and device vendors
  - 110 companies and growing



Src: UCIe Consortium

Chiplet Ecosystem Challenges

- Standard integration model for all functions
  - Protocol/Electrical/Physical
  - Software/firmware
  - Security & Manageability
  - Debug and Test
  - Power/Thermal/RAS
- Additional challenges
  - Logistics
  - Mixing Foundries
  - System Test



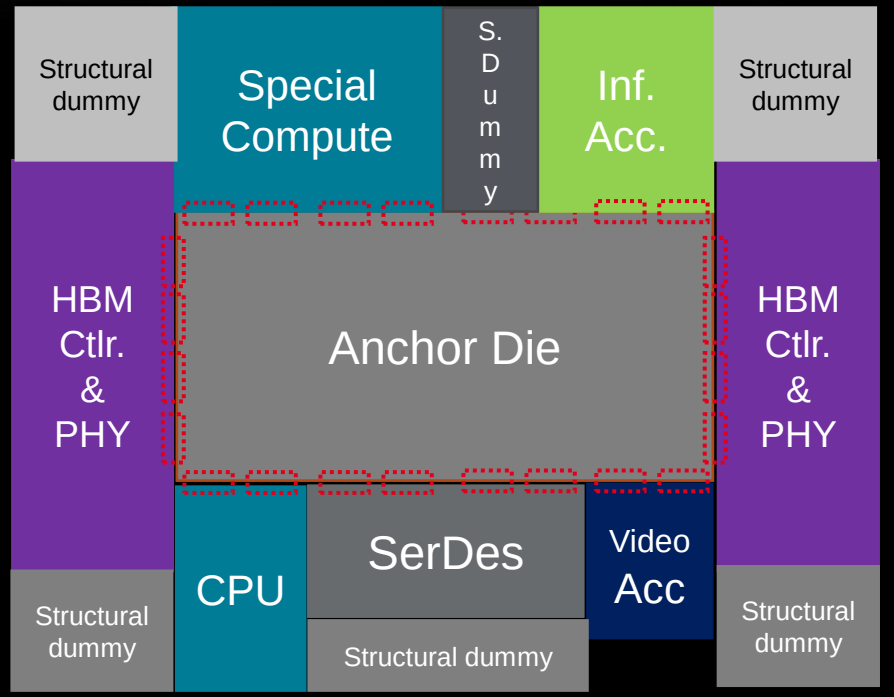
Chiplet Attach/Usage Model

- Pcie/CXL device (well established)
  - Software/driver
  - Address translation
  - Error isolation and recovery
  - Use Case: Inference, video, crypto, compression or networking functions acceleration

- Memory Controller+PHY chiplets
  - Simple protocol desired for standardization
  - Streaming protocol supported for proprietary use case
  - Use Case: Flexible memory technology (HBM / DDR / LPDDR / G6 /..)

- Generic compute attach
  - HMM or other memory management instead of device ATS/ATC
  - Standard coherency architecture like CXL (simplified) or CHI
  - Holy Grail ?? Needs work and alignment in consortium

- SerDes I/O chiplets
  - Use case: Pcie 32G/64G/128G ; Ethernet 50G/100G/200G



Chiplet Footprint

- PCIe has several detailed Card Electro-Mechanical specifications
  - Defines sizes, speed and power requirements
  - CEM AIC, M.2 and U.2

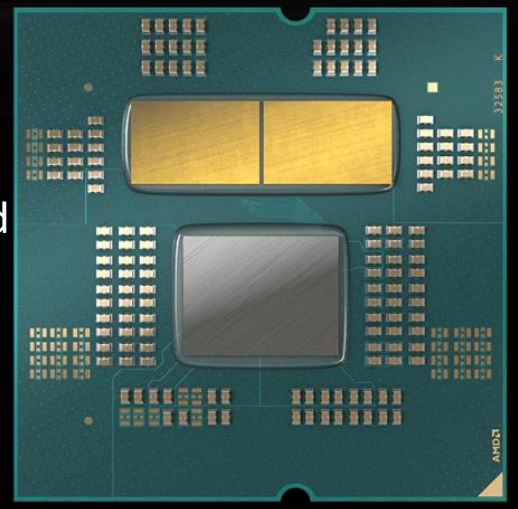
- Chiplets also need form factor standards
  - Power, Width & Height
  - Links (BW), Beach front & Alignment
  - Etc.

- System In a Package(SiP) has significantly reduced flexibility than add-in cards
  - Standard Packages are more a bit more flexible than AP

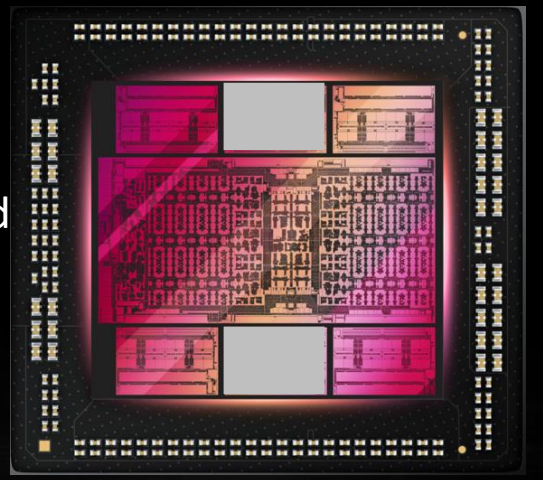
- Structural dies may be required when there are holes or gaps between chiplets

- Form factor standardization is crucial for a chiplet ecosystem!

Standard Package



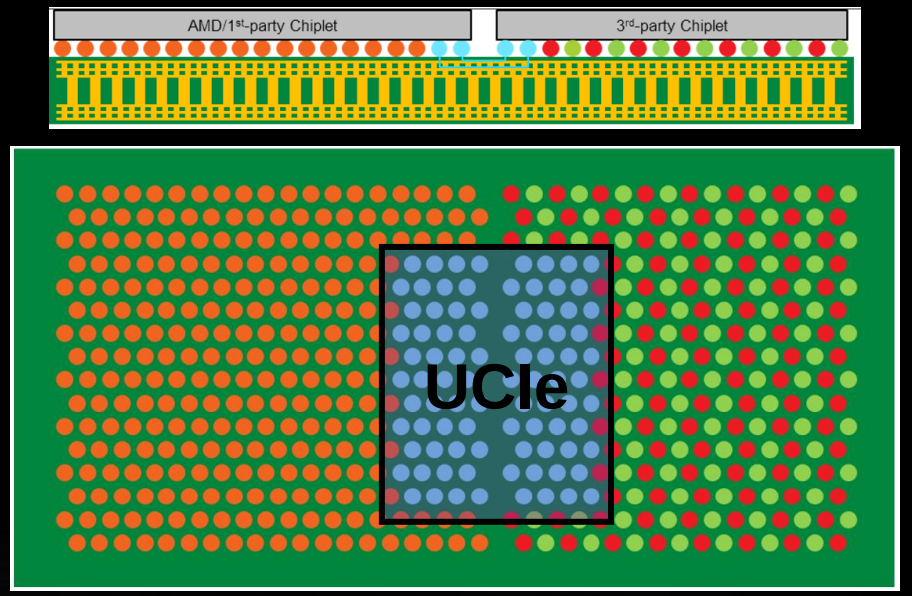
Advanced Package



Package Resources & Impact

- Typically, many package resources are allocated for external IO and logic power delivery
- Chiplet interconnects are
  - Buried deep in the interior of the dies
  - Designed to be small (and coexist with SoC Logic)
  - Ideal chiplet interconnects will leverage available digital supplies
  - Chiplets expected to be deployed in harsh environments
  - Operating on noisy supplies, pushes solutions to be wide and slow
- UCIe allows multi-module(ganged) configurations for higher bandwidth
- Need good measurement and debug capabilities

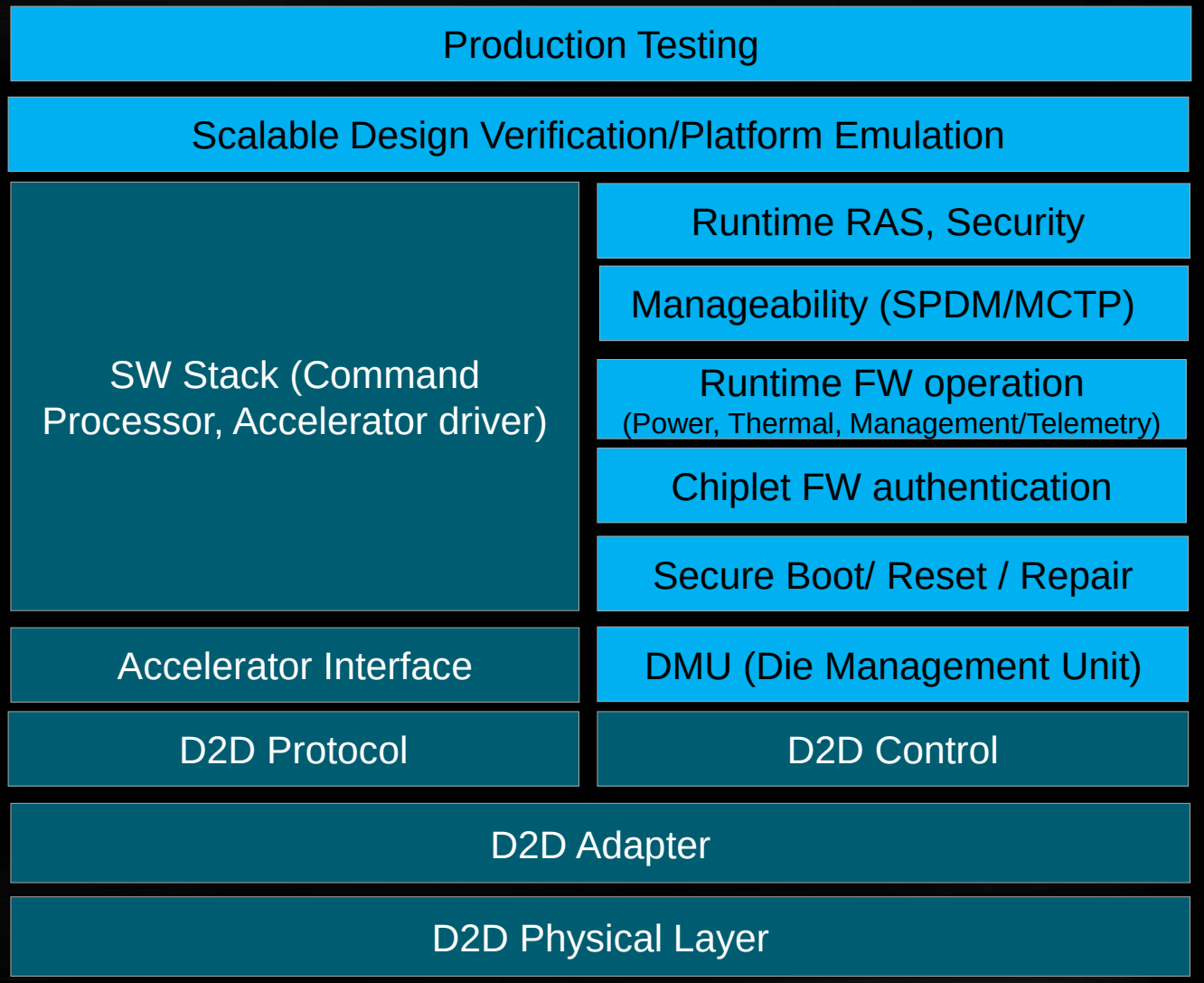
UCIe only defines interconnect beach front
Power Delivery and DFX pins equally important



Chiplet Ecosystem Solution Stack

PCIE/CXL DEVICE INTEGRATION MODEL

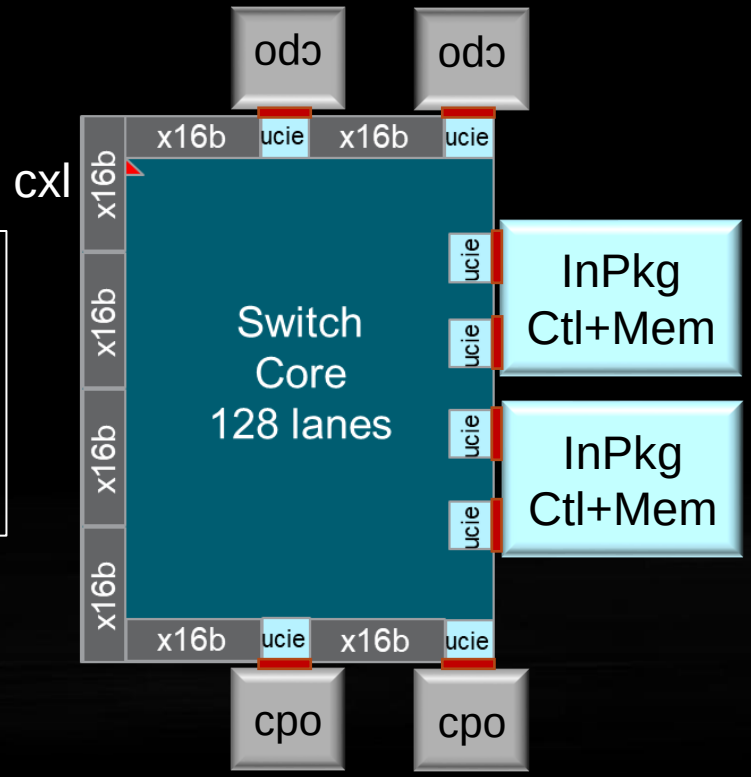
- Two independent hardware stack
  - Protocol and Control
- Die management unit (DMU)
  - Hardware + Firmware
- Standard control and management software interface
- Platform specific firmware
- UCIe starting to tackle software interfaces

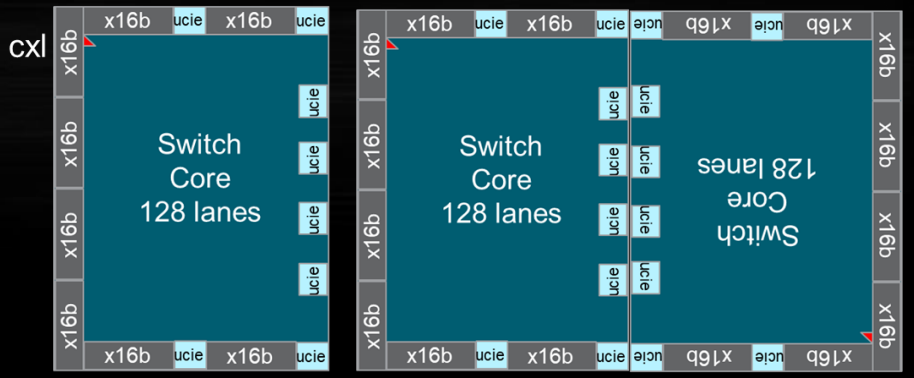


Chiplet Applications

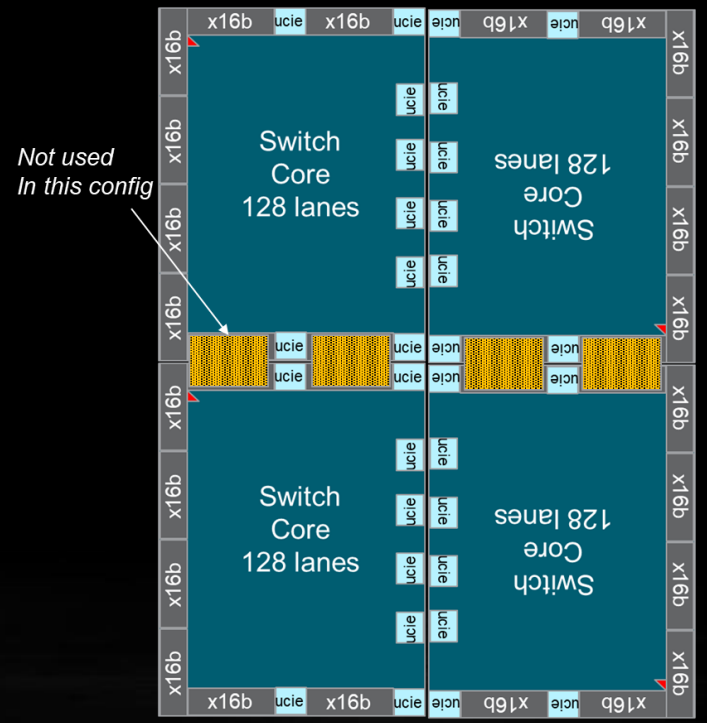
- Scalable CXL switch for illustration
  - Cost benefits due to standardized bridge chips
  - Flexibility to add
    - co-packaged optics
    - in-package memory
  - Many product options with a single die

128 lanes electrical
128 lanes equivalent optical
In-package memory





Small (128 lanes) Medium (256 lanes)



Large (384 lanes)

Summary

- Wide adoption of standard is critical
  - UCIe clears the bar with over 110 companies within 6 months of incorporation
  - UCIe on a path to enable multiple protocols – CXL, AXI, etc.
- Pcie/CXL device integration model is well established
- Critical for partners to collaborate closely
- May need custom solutions to kick start ecosystem
- Chiplets are here but will take a few years for an ecosystem

Acknowledgements

- Alex Branover, Senior Fellow, AMD (alex.branover@amd.com)
- Anwar Kashem, Sr. Fellow/CVP, AMD (anwar.kashem@amd.com)

Disclaimer and copyright

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions, and typographical errors. The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. Any computer system has risks of security vulnerabilities that cannot be completely prevented or mitigated. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

This information is provided "as is." AMD makes no representations or warranties with respect to the contents hereof and assumes no responsibility for any inaccuracies, errors, or omissions that may appear in this information. AMD specifically disclaims any implied warranties of non-infringement, merchantability, or fitness for any particular purpose. In no event will AMD be liable to any person for any reliance, direct, indirect, special, or other consequential damages arising from the use of any information contained herein, even if AMD is expressly advised of the possibility of such damages.


AMD